UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,960	09/26/2003	Kourosh Gharachorloo	200302257-2	9440

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EXAMINER
CHERY, MARDOCHEE

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/672,960	GHARACHORLOO ET AL.
	Examiner	Art Unit	
	Mardochee Chery	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2003*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6 and 11-21* is/are rejected.

7)☒ Claim(s) *3 and 7-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☐ All   b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
     Paper No(s)/Mail Date *9/26/03*.

4) ☐ Interview Summary (PTO-413)
     Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1.   The present Office action is a Non-Final Office Action resulting from examination and search of claims 1-21 of the instant application. Applicant is reminded that each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in 37 CFR 1.56.

Claim Objections

2.   Claims 2, 5, and 10 are objected to because of the following informalities:

a.   In claim 2, line 6, "each node identifier stored in the identification field occupies *of* plurality of bits" should be changed to -- each node identifier stored in the identification field occupies *a* plurality of bits--.

b.   In claim 5, line 4, "*the first number* is greater than *the first number*" should be changed. In the current Office Action, this limitation is interpreted as --the second number is greater than the first number--.

c.   In claim 10, line 2, "the protocol engine is configured send a respective version" should be changed to -- the protocol engine is configured *to* send a respective version--.

Appropriate correction is required.

Double Patenting

3.   Claims 1-2, 4-6, and 11-21 of U.S. Patent No. 6,697,919 contains every element

of claim 1-20 of the instant application and as such provisionally anticipates claim 1-20

of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the

later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at

896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting

because the claims at issue were obvious over claims in four prior art patents); In re

Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of

obviousness-type double patenting where a patent application claim to a genus is

anticipated by a patent claim to a species within that genus). " ELI LILLY AND

COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the

Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30,

2001).

This is an obviousness-type double patenting rejection because the conflicting

claims have not in fact been patented.

4.   The following table is provided to demonstrate the relationship between the

conflicting claims. Claim 1 is used for illustrative purposes only:

Instant App. 10/672,960	U.S. Patent No. 6,697,919
1. A multiprocessor computer system,	**1.** A multiprocessor computer system,

comprising:	comprising:
a plurality of nodes, each node including:	a plurality of nodes, each node including:
an interface to a local memory subsystem, the local memory subsystem storing a multiplicity of memory lines of information and a directory;	an interface to a local memory subsystem, the local memory subsystem storing a multiplicity of memory lines of information and a directory;
a memory cache for caching a multiplicity of memory lines of information, including memory lines of information stored in a remote memory subsystem that is local to another node;	a memory cache for caching a multiplicity of memory lines of information, including memory lines of information stored in a remote memory subsystem that is local to another node;
the directory including an entry associated with a memory line of information stored in the local memory subsystem, the entry including an identification field for identifying a subset of nodes from the plurality of nodes caching the memory line of information;	the directory including an entry associated with a memory line of information stored in the local memory subsystem, the entry including an identification field for identifying a subset of nodes from the plurality of nodes caching the memory line of information;
the identification field configured to comprise a plurality of bits at associated	the identification field configured to comprise a plurality of bits at associated

positions within the identification field;	positions within the identification field;
a protocol engine implementing a cache coherence protocol, said protocol engine configured to associate with each respective bit of the identification field one or more nodes of the plurality of nodes, including a respective first node, wherein the one or more nodes associated with each respective bit are determined by reference to the position of the respective bit within the identification field;	a protocol engine implementing a cache coherence protocol, said protocol engine configured to associate with each respective bit of the identification field one or more nodes of the plurality of nodes, including a respective first node, wherein the one or more nodes associated with each respective bit are determined by reference to the position of the respective bit within the identification field;
set each bit in the identification field of the directory entry associated with the memory line for which the memory line is cached in at least one of the associated nodes;	set each bit in the identification field of the directory entry associated with the memory line for which the memory line is cached in at least one of the associated nodes;
send an initial invalidation request to no more than a first predefined number of the nodes associated with set bits in the identification field of the directory entry associated with the memory line.	send an initial invalidation request to no more than a first predefined number of the nodes associated with set bits in the identification field of the directory entry associated with the memory line.

Claim Rejections - 35 USC § 102

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6.   Claims 1, 2, 4-6, 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated

by Computer Architecture: A Quantitative Approach by Patterson Hennessey.

With respect to claim 1, Patterson and Hennessy teach a multiprocessor

computer system [Fig. 8.22, pp 680]; comprising a plurality of nodes, each node

including an interface to a local memory subsystem, a cache memory, and a directory.

Patterson and Hennessy (pp 679-680, 682-683) also disclose a directory-based cache

coherence protocol, along with a bit vector, wherein the vector includes bits for state

information (shared, uncached, and exclusive), bits associated with the owner of the

block, and a bit associated with each processor that has a copy of that corresponding

memory block (i.e. the shares); a protocol engine implementing a cache coherence

protocol configured to associate with each respective bit of the identification field one or more nodes of the plurality of nodes determined by reference to the position of the respective bit within the identification field (pp 679, 681). Additionally, an invalidation request can be made to a specific number of nodes (the sharers) associated and predefined by the set bits in the bit vector (pp 683-685).

Regarding claims 2 and 4, Patterson and Hennessey teach node identifiers in the identification field having a plurality of bits (e.g. state field: shared, uncached, or exclusive) that identify a subset of the plurality of nodes. In the teachings of Patterson and Hennessey, the second predefined number of nodes could be interpreted as the total number of nodes or bits in the bit vector. Patterson and Hennessey also teach that the invalidation request is sent to the first subset, the "sharers" (pp 680-685), predefined by the setting of each bit to "1".

Regarding claim 5, Patterson and Hennessey teach the use of a bit vector (pp 680), including a plurality of bits associating each node with a bit ("second number"). A plurality of nodes with a bit set in the bit vector indicates the number of nodes sharing the memory block ("first number"). The second number could be greater than the first. In this instance, the protocol associates each respective node (whether it be the first, second, third...or the nth node) with a particular node identifier, corresponding to one of the bits in the bit vector.

Regarding claim 6, Patterson and Hennessey also teach a first node associated with the set bit receiving an invalidation request from the protocol (pp 680-685).

Regarding claim 16, Patterson and Hennessey disclose (pp 680-685) a respective subset of bits (e.g., bits used to either identify owner of the block or bits used to identify a state such as the exclusive state are able to associate one node within the subset of sharer nodes) configured to associate one node within the subset when the subset of nodes includes fewer than a second predefined number of nodes (e.g., total number of nodes or bits in the bit vector).

Regarding claim 17, Patterson and Hennessey also teach the use of bits to track the state of each cache block (e.g., pp 679-681).

Regarding claim 18, Patterson and Hennessey teach (pp 680-685) a respective subset of bits (e.g., bits used to either identify owner of the block or bits used to identify a state such as the exclusive state are able to associate one node within the subset of sharer nodes) configured to associate one node within the subset when the subset of nodes includes fewer than a second predefined number of nodes (e.g., total number of nodes or bits in the bit vector).

7.   Claims 19-21 rejected under 35 U.S.C. 102(e) as being anticipated by Safranek

(US 6,493,809).

        With respect to claims 19-21, Safranek teaches a protocol engine implementing a

cache coherence protocol, for use in a multiprocessor system (e.g., Fig. 2), the protocol

engine located at a particular node of a plurality of nodes, the protocol engine (e.g., Fig.

4) comprising: input logic for receiving a first invalidation request (e.g., col. 8, ll 61 to col.

12) the invalidation request identifying a memory line of information and including a

pattern of bits for identifying a subset of the plurality of nodes that potentially store

cached copies of the identified memory line; and processing circuitry, responsive of

receipt of the first invalidation request for sending a second invalidation corresponding

to the first invalidation request to a next node if the plurality of bits in fact identifying the

next node (e.g., col. 8, ll 61 to col. 12); sending an invalidation acknowledgment (e.g., a

response) to a requesting node identified in the first invalidation message if the plurality

of bits fail to identify a next node (e.g., response to indicate that it is complete; col. 8, ll

61 to col. 12); and invalidating a cached copy of the identified memory line, if any, in the

particular node of the plurality of nodes in the multiprocessor system.

Claim Rejections - 35 USC § 103

8.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9.   Claims 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Computer Architecture: A Quantitative Approach by Patterson and Hennessey in view of Safranek (US 6,493,809).

Regarding claims 11 and 15, Patterson and Hennessey teach the limitations of claim 1, but do not specifically teach that the protocol includes in the initial invalidation request a pattern of bits such that the recipient node of the initial invalidation request can derive from the pattern of bits of a next recipient node, if any, to which to send a second invalidation request corresponding to the initial invalidation request. Safranek, however, teaches a method of invalidating shared cache lines by using a protocol, wherein the invalidate request is sent from the head node to a succeeding node (recipient node) on the sharing list and continuously in a doubly linked list format until the last recipient node has recipient the request (e.g., col. 8, ll 61 to col. 12). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Safranek with Patterson and Hennessey because Safranek provides a particular method that can be used to invalidate a request and specifically states that the method is "useful in multiprocessor systems such as a distributed shared memory (DSM) or non-uniform memory access (NUMA) machines that include a number of interconnected processor nodes each having local memory and caches that store copies of the same data " (Safranek; Abstract) and may be used with various types of protocols (e.g., Safranek: col. 12, ll 55-67), as described by

Patterson and Hennesey. The combination of the two teachings would reduce the time

for invalidating cache lines on a sharing list by performing some of the requisite actions

in parallel.

10.   Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Computer Architecture: A Quantitative Approach by Patterson and Hennessey in view of

Laudon (US 5,634,110).

Regarding claim 12, Patterson and Hennessey discloses the limitations of claim

1, but do not specifically mention that the identification field is subdivided to form a

number of groups of bits and to send an initial invalidation request to a first node, if any,

associated with a set bit in the respective group of bits. Laudon, however, disclose a

modified coarse bit vector format (e.g., col. 7, ll 30 to col. 8, ll 57), which includes an

identification field that is subdivided. An initial invalidation request would then be sent to

a first node associated with a set bit along with a pattern of bits. Thus, it would have

been obvious to one of ordinary skill in the art at the time of invention by applicant to

combine the teachings of Patterson and Hennessey with Laudon because Laudon

discloses particular types of bit vector formats that can be used for cache coherency in

a distributed computing environment as described by Patterson and Hennessey. The

combination of the teachings would provide for different vector bit types that results in

minimal if any directory storage overhead.

Regarding claims 13 and 14, in the system of Patterson and Hennessey, the protocol send s the invalidation request to all the nodes with a set bit (pp 682-685). Thus, if the node of the second is set, an invalidation request will be sent to the second node.

Allowable Subject Matter

11.   Claims 3, and 7-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
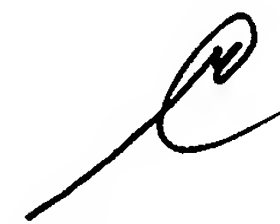
Conclusion

12.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mardochee Chery whose telephone number is (571)272-4246. The examiner can normally be reached on 8:30A-5:00P.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manonama Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
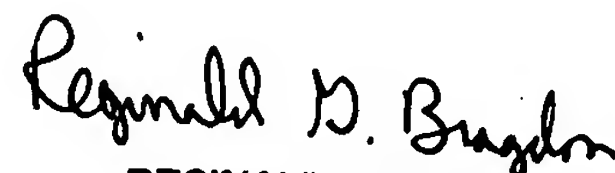
Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

September 7, 2006

Mardochee Chery
Examiner
AU: 2188

REGINALD BRAGDON
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100